CLAIMS

1. A test system comprising:

a test wafer having a plurality of dies to be tested and a first set of pads exposed in a first pattern at a first surface of the test wafer, the first set of pads providing electrical connections to the dies;

a probe wafer having an auxiliary test circuit, a second set of pads exposed in a second pattern at a first surface of the probe wafer, a third set of pads exposed in a third pattern at a second surface of the probe wafer, and an interconnect structure for connecting the auxiliary test circuit, the second set of pads and the third set of pads;

a prober configured to align the first set of pads of the test wafer with the second set of pads of the probe wafer, place the first set of pads of the test wafer into contact with the second set of pads of the probe wafer.

2. The test system of Claim 1, wherein the prober further comprises a set of probe needles configured to contact the third set of pads at the second surface of the probe wafer.

3. The test system of Claim 2, further comprising a tester, wherein the prober includes means for coupling the tester to the probe needles.

4. The test system of Claim 1, wherein each of the dies includes a non-volatile memory array.

5. The test system of Claim 1, wherein the auxiliary test circuit includes a plurality of test circuits, each being coupled to a corresponding die on the test wafer.

6. The test system of Claim 1, wherein the test wafer further comprises a plurality of built-in self-test (BIST) circuits, which are coupled to the auxiliary test circuit in probe wafer.

7. The test system of Claim 6, wherein each of the dies has a corresponding BIST circuit.

8. The test system of Claim 6, wherein the ratio of the dies to the BIST circuits is 100:1 to 1000:1.

9. The test system of Claim 6, wherein the BIST circuits are located in scribe-line areas or drop-in areas of the test wafer.

10. The test system of Claim 1, wherein the probe wafer further comprises a plurality of electrically conductive studs located on the second set of pads, wherein the conductive studs contact the first set of pads on the test wafer when the probe wafer is coupled to the test wafer.

11. The test system of Claim 1, wherein the interconnect structure of the probe wafer extends around edges of the probe wafer.

12. The test system of Claim 1, wherein the interconnect structure of the probe wafer extends through

the probe wafer, between the first surface of the probe wafer and the second surface of the probe wafer.

13. The test system of Claim 1, wherein the auxiliary test circuit comprises circuitry for performing a read/verify operation in the test wafer.

14. The test system of Claim 1, wherein the auxiliary test circuit comprises circuitry for performing a program operation in the test wafer.

15. The test system of Claim 1, wherein the auxiliary test circuit comprises circuitry for performing an erase operation in the test wafer.

16. The test system of Claim 1, wherein the substrate comprises a monocrystalline semiconductor material.

17. The test system of Claim 1, wherein the prober further comprises means for aligning the probe wafer and the test wafer.

18. The test system of Claim 17, wherein the means for aligning comprise an optical alignment system.

19. The test system of Claim 18, further comprising optical alignment marks on the test wafer and the probe wafer.

20. The test system of Claim 17, wherein the means for aligning comprise a mechanical alignment system.

21. The test system of Claim 20, further comprising alignment holes formed through the probe wafer.

22. The test system of Claim 20, wherein the test wafer and the probe wafer have the same size and shape.

23. The test system of Claim 1, wherein the test wafer is a wafer level chip scale packaged (WLCSP) wafer.

24. A method for testing a plurality of dies located on a test wafer, the method comprising:

coupling the test wafer to a probe wafer, such that a set of pads on the test wafer is placed into contact with a first set of pads on a first surface of the probe wafer;

coupling a prober to a second set of pads on a second surface of the probe wafer, opposite the first surface;

transmitting a first set of test signals from the prober to the second set of pads of the probe wafer;

transmitting the first set of test signals from the second set of pads to test circuitry fabricated on the probe wafer;

generating a second set of test signals in response to the first set of test signals using the test circuitry; and

transmitting the second set of test signals from the test circuitry on the probe wafer to the test wafer through the first set of pads on the probe wafer and the set of pads on the test wafer.

25. The method of Claim 24, further comprising:

generating a third set of test signals in response to the second set of test signals using the dies on the test wafer; and

transmitting the third set of test signals to the test circuitry on the probe wafer.

26. The method of Claim 25, wherein the third set of test signals are further generated using built-in self-test (BIST) circuits located on the test wafer.

27. The method of Claim 24, wherein the step of coupling the test wafer to the probe wafer further comprises optically aligning the test wafer and the probe wafer.

28. The method of Claim 24, wherein the step of coupling the test wafer to the probe wafer further comprises mechanically aligning the test wafer and the probe wafer.

29. A probe wafer comprising:

a substrate;

test circuitry fabricated on the substrate;

an interconnect circuit coupled to the test circuitry;

a first set of pads coupled to the interconnect circuit at a first surface of the substrate, the first set of pads having a pattern to correspond with a pattern of pads on a test wafer;

a second set of pads located on a second surface of the substrate, wherein the second surface is opposite the first surface; and

a plurality of traces coupling the first set of pads to the second set of pads.

30. The probe wafer of Claim 29, wherein a first set of the traces extend around outer edges of the substrate.

31. The probe wafer of Claim 30, wherein a second set of traces extend through the substrate.

32. The probe wafer of Claim 29, wherein a set of the traces extend through the substrate.

33. The probe wafer of Claim 29, wherein the test circuitry comprises a first set of registers for storing a first set of test data values to be written to a test wafer.

34. The probe wafer of Claim 33, wherein the test circuitry further comprises a second set of registers for storing a second set of test data values read from the test wafer.

35. The probe wafer of Claim 34, wherein the test circuitry further comprises a set of comparators for comparing the first set of test data values with the second set of test data values.

36. The probe wafer of Claim 29, wherein the test circuitry comprises circuitry for performing a read/verify operation in the test wafer.

37. The probe wafer of Claim 29, wherein the test circuitry comprises circuitry for performing a program operation in the test wafer.

38. The probe wafer of Claim 29, wherein the test circuitry comprises circuitry for performing an erase operation in the test wafer.

39. The probe wafer of Claim 29, wherein the substrate comprises a monocrystalline semiconductor material.

40. The probe wafer of Claim 39, wherein the substrate comprises silicon.

41. The probe wafer of Claim 29, wherein the substrate comprises a ceramic or glass material.

42. The probe wafer of Claim 29, further comprising a plurality of electrically conductive studs formed on the first set of pads.

43. The probe wafer of Claim 29, wherein the test circuitry includes a plurality of test circuits, wherein each test circuit corresponds with a die in the test wafer.